Abstract of the Disclosure

Improved semiconductor integrated circuit random access memory (RAM) features pin-compatible replacement of SRAM devices, while providing low power and high density characteristics of DRAM devices. The refresh operations of a DRAM array are hidden so as to faithfully emulate an SRAM-type interface. The new refresh strategy is based on prohibiting the start of a refresh operation during certain periods but otherwise continuously refreshing the array, rather than affirmatively scheduling refresh at certain times as in the prior art. Short refresh operations are initiated frequently, driven by an internal clock that generates periodic refresh requests, except when a read or write operation is actually accessing the memory array. By isolating the DRAM memory array from I/O structures, external memory accesses are essentially interleaved with refresh operations, rather than temporally segregating them as in prior art.